What is claimed as new and desired to be protected by Letters Patent of the United States is:

Sub A1

1. A method of providing clocking signals over a bus, said method comprising:

providing a first clock signal which travels over a first conductive path of said bus in a first direction;

providing a second clock signal which travels over a second conductive path of said bus in a second direction opposite to said first direction; and

causing said first and second clock signals to have a predetermined phase relationship with respect to each other at a predetermined location on said bus.

2. A method of claim 1 wherein said predetermined phase relationship is substantially an in-phase relationship.

3. A method as in claim 1 or 2 wherein said act of causing comprises detecting the phase relationship of said first and second clock signals at said predetermined location and adjusting at least one of said first and second clock signals to obtain said predetermined phase relationship.

Sub A1

4. A method as in claim 1 or 2 wherein said act of causing comprises configuring the signal propagation characteristics of at least one of said first and second conductors to obtain said predetermined relationship.

5. A method as in claim 4 wherein said act of configuring comprises configuring the path length of said first and second conductors to obtain said predetermined phase relationship.

6. A method as in claim 3 wherein one of said clock signals is a data write clock signal and the other of said clock signals is a data read clock signal.

7. A method as in claim 3 wherein a plurality of input/output devices are connected to said bus at spaced locations, said first and second clock signals being supplied to said devices, and wherein said predetermined location is along the length of said first and second conductors between locations where said first and second conductors supply said first and second clock signals to said input/output devices.

8. A method as in claim 7 wherein said predetermined location is substantially midway of said locations where said first and second conductors supply said first and second clock signals to said input/output devices.

Sub A1

9. A method as in claim 7 wherein each of said input/output devices comprise a memory subsystem and one of said first and second clock signals is a data write clock signal, and the other of said first and second clock signals is a data read clock signal.

10. A method as in claim 9 wherein said data write and data read signals have the same clock period and wherein said memory subsystems are spaced along said bus and said predetermined phase relationship and distance of said memory modules from said predetermined location is such that the phase deviation of said data write and data read clock signals at any one of said memory subsystems is less than one half of a data bit time.

11. A method as in claim 10 wherein said memory subsystems are equally spaced along said bus.

12. A method as in claim 9 wherein each of said memory subsystems comprises a plurality of memory storage devices, and said method further comprises receiving a data write clock signal at said memory subsystem, regenerating a plurality of data clock write signals from a received data write clock signal, and respectively providing said plurality of regenerated data write signals to said plurality memory storage devices.

13. A method as in claim 10 wherein each of said plurality of regenerated data write clock signals are substantially in phase with each other.

Sub A1

14. A method as in claim 13 wherein each of said plurality of regenerated data write clock signals at said memory storage devices of an associated memory subsystem are substantially in phase with a write clock signal received at said associated memory subsystem.

15. A method as in claim 9 wherein each of said memory subsystems comprises a plurality of memory storage devices and said method further comprises receiving a data read clock signal, regenerating a plurality of data read signals from said received data read clock signal and respectively providing said plurality of regenerated data read clock signals to said plurality of memory storage devices.

16. A method as in claim 15 wherein said plurality of regenerated data read signals are regenerated inside a device which produces the data write clock signal and data read clock signal.

17. A method as in claim 15 wherein said regeneration of said data read clock signals occurs at a motherboard which contains said bus.

Sub A1

18. A method as in claim 15 wherein one of said plurality of regenerated data read clock signals is used in said act of detecting said phase relationship.

19. A method as in claim 15 wherein said each of said plurality of regenerated data read clock signals are in phase with each other.

20. A method as in claim 19 wherein each of said plurality of regenerated data read clock signals are in phase with said received data read clock signal.

21. A method as in claim 6 wherein said bus interconnects a memory controller with at least one memory subsystem, said memory controller, issuing said data write clock signal and said data read clock signal on said first and second conductive paths, detecting said phase relationship of said data write clock signal and data read clock signal at said predetermined location, and adjusting the timing of at least one of said data write signal and said data read clock signal to obtain said predetermined phase relationship at said predetermined location.

22. A method as in claim 21 wherein the conductive path over which said data write clock signal passes is terminated at and end thereof spaced from an

said memory controller, said memory subsystem being located between said controller and the terminated end of said data write clock signal conductive path.

Sub #1

23. A method as in claim 21 wherein the path over which said data read clock signal passes is a loop back conductive signal path.

24. A method as in claim 23 wherein said loop back conductive signal path is terminated at an end thereof.

25. A method as in claim 23 wherein said loop back conductive signal path terminates at both ends at said memory controller.

26. A method as in claim 21 wherein said memory controller generates said data read clock signal off said date write clock signal.

27. A method as in claim 26 wherein said memory controller adjusts a phase relationship between said data write clock signal and data read clock signal using a phase lock loop or delay lock loop which sets a phase relationship between said data write clock signal and data read clock signal at said predetermined location.

28. A method as in claim 27 further comprising receiving at said phase lock loop feedback signals representing the relative phase relationship of

Sub A1

said data write clock signal and data read clock signal at said predetermined location and using said relative phase relationship to adjust the phase relationship of said data write clock signal and data read clock signal at said predetermined location.

29. A method as in claim 9 wherein said memory subsystem comprises a plurality of memory storage devices and is connected over said bus to a memory controller, said memory controller issuing a data write clock signal which is received at said memory subsystem, said method further comprising regenerating a plurality of data write clock signals from a received data write clock signal and respectively providing said regenerated data write clock signals to said memory storage devices.

30. A method as in claim 29 further comprising issuing a plurality of data read clock signals from said memory controller which are received at said memory subsystem and respectively providing said received data read clock signals to said memory storage devices.

31. A method as in claim 29 further comprising issuing a data read clock signal from said memory controller and regenerating from said issued data read clock signal a plurality of regenerated data read clock signals and respectively

Sub A1

applying said plurality of regenerated data read clock signals to said memory storage devices.

32. A method as in claim 31 wherein regeneration of said data read clock signals is performed at a motherboard which contains said bus.

33. A method as in claim 9 wherein said memory subsystems are spaced along said bus such that when a data read clock signal and a data write clock signal are received thereat a predetermined minimum time exists between them.

34. A method as in claim 33 wherein said predetermined minimum time is such that a data read clock signal does not arrive at a said memory subsystem during a period of time following initialization of a data write signal, said period of time being about 50% of the period of the data write clock signal.

35. A method as in claim 32 wherein at least one of said regenerated data read signals is used in said phase relationship determination.

36. A method as in claim 29 wherein said memory subsystem includes a register for receiving command and address data from command and address paths of said bus, said method further comprising providing command and address data to said memory storage devices, regenerating an additional data

Sub A1

write clock signal from said received data write clock signal, and using said additional regenerated data write clock signal to control the capture of command and address data within said register.

37. A method as in claim 36 wherein the frequency of said additional data write clock signal is at a frequency of X/N where X is the frequency of said received data write clock signal and N is an integer.

38. A method as in claim 9 wherein said memory subsystem is a memory module which is capable of being socket connected to said bus.

39. A method as in claim 9 wherein each memory subsystem comprises a plurality of memory storage devices, said method further comprising issuing a data ready signal from at least one of said memory storage devices onto said bus when said plurality of memory storage devices are about to place data on said bus.

40. A method as in claim 9 wherein each memory subsystem is coupled to a memory controller over said bus and each memory subsystem comprises a plurality of memory storage devices, said method further comprising calibrating the turn on time of data receivers in said memory controller using a known data pattern contained in at least one of said memory storage devices.

Sub A1

41. A method as in claim 40 wherein said act of calibrating comprises writing said known data pattern to said at least one memory storage device, issuing a read command to said at least one memory storage device from said memory controller, detecting an aligning edge of said known data pattern at said memory controller and determining the time between the issuance of said read command and the aligning edge of said known data pattern and using said determined time difference to turn on data receivers in said memory controller following issuance of a read command.

42. A clock system for a data bus, comprising:

a data bus comprising:

a plurality of data paths;

a first clock signal path for propagating a first clock signal in a first direction along said bus;

a second clock signal path for propagating a second clock signal in a second direction opposite to said first direction along said bus;

a bus controller for issuing said first and second clock signals in said first and second clock signal paths; and

Sub A1

circuitry for causing said first and second clock signals to have a predetermined phase relationship with respect to each other at a predetermined location along said bus.

43. A system as in claim 42 wherein said predetermined phase relationship is substantially an in-phase relationship.

44. A system as in claim 42 wherein said circuitry comprises the signal propagating characteristics of said first and second clock signal paths.

45. A system as in claim 44 wherein said circuitry includes the path lengths of said first and second clock signal paths.

46. A system as in claim 42 wherein said circuitry is a phase detecting circuit associated with said bus controller, said phase detecting circuit detecting the phase relationship of said first and second clock signals at said predetermined location and adjusting at least one of said first and second clock signals to obtain said predetermined phase relationship.

47. A system as in claim 46 wherein one of said clock signals is a data write clock signal and the other clock signal is a data read clock signal.

Sub A1

48. A system as in claim 47 further comprising a plurality of data input/output devices coupled to said bus, said input/output devices receiving said data write clock signal and said data read clock signal.

49. A system as in claim 42 wherein said predetermined location is at a location along the length of said first and second conductors between first and second locations where said first and second conductors supply said first and second clock signals to said input/output devices.

50. A system as in claim 49 wherein said predetermined location is substantially the midpoint of said first and second locations.

51. A system as in claim 49 wherein each of said input/output devices comprise a memory subsystem and one of said first and second clock signals is a data write clock signal, and the other of said first and second clock signals is a data read clock signal.

52. A system as in claim 51 wherein said data write and data read clock signals have the same clock period and wherein said memory subsystems are spaced along said bus and said predetermined phase relationship and distance of said memory modules from said predetermined location is such that the phase

deviation of said data write and data read clock signals at any one of said memory subsystems is less than one half of a data bit time.

Sub A1

53. A system as in claim 52 wherein said memory subsystems are equally spaced along said bus.

54. A system as in claim 51 wherein each of said memory subsystems comprises a plurality of memory storage devices, said system further comprising a data write regeneration circuit which regenerates a plurality of data write clock signals from a received data write clock signal and respectively supplies said regenerated data write clock signals to said memory storage devices.

55. A system as in claim 54 wherein said plurality of regenerated data write clock signals are in phase with each other.

56. A system as in claim 55 wherein said plurality of regenerated data write clock signals at said memory storage devices are in phase with said data write clock signal received at an associated memory subsystem.

57. A system as in claim 54 wherein said data write clock generating circuit comprises a plurality of buffer circuits for respectively providing said plurality of regenerated data circuit clock signals.

Sub A1

58. A system as in claim 54 wherein said data write clock regenerating circuit comprises a phase lock loop circuit.

59. A system as in claim 51 wherein each of said memory subsystems comprises a plurality of memory storage devices, said system further comprising a circuit for regenerating a plurality of data read clock signals and respectively providing said plurality of regenerated data read clock signals to said plurality of memory storage devices.

60. A system as in claim 59 wherein said circuit for regenerating said data read clock signals is located at a motherboard which contains said bus.

61. A system as in claim 60 wherein said regenerated read data clock signal is generated inside a transmitting device which generates said data write clock signal and data read clock signal.

62. A system as in claim 60 further comprising a phase detector associated with said bus controller for detecting the phase relationship of said data write clock signal at said predetermined location and adjusting at least one of said write clock signals and read clock signals to obtain said predetermined relationship.

Sub A1

63. A system as in claim 62 wherein at least one of said plurality of regenerated data read signals is used by said phase detector to detect said phase relationship.

64. A system as in claim 59 wherein said each of said plurality of regenerated data read clock signals are in phase with each other.

65. A system as in claim 64 wherein each of said plurality of regenerated data read clock signals are in phase with said received data read clock signal.

66. A system as in claim 59 wherein said circuit for regenerating said plurality of data read clock signals comprises a plurality of buffer circuits.

67. A system as in claim 59 wherein said circuit for regenerating said plurality of data read clock signals comprises a PLL circuit.

68. A memory system comprising:

a data bus comprising a plurality of read/write data paths, a data write clock signal path for propagating a data write clock signal in a first direction along said bus, and a data read clock signal path for propagating a data read clock

Sub A1

signal in a second direction along said bus, said second direction being opposite said first direction;

a memory controller coupled to said bus for respectively issuing said data write and data read clock signals on said data write and data read clock signal paths and for setting a predetermined phase relationship between said data write and data read clock signals at a predetermined location along said bus; and

at least one memory subsystem coupled to said bus for exchanging data with said memory controller in accordance with timing set by said data write and data read clock signals.

69. A memory system as in claim 68 wherein each said memory subsystem comprises a plurality of memory devices which transmit data to and receive data from said data bus in accordance with said timing set by said data write and data read clock signals.

70. A memory system as in claim 69 further comprising a plurality of memory subsystems coupled to said bus at spaced locations therealong, said predetermined location being located between a first location where a memory subsystem which is nearest to said memory controller is coupled to said bus and a

second location where a memory subsystem which is farthest from said memory controller is coupled to said bus.

Sub #1

71. A memory system as in claim 70 wherein said predetermined location is located substantially midway of said first and second locations.

72. A memory system as in claim 68 wherein said memory controller has an associated phase lock loop circuit for maintaining said predetermined phase relationship, said phase lock loop or delay lock loop circuit receiving data write and data read clock signals from said predetermined location as inputs and providing an output which adjusts the phase relationship of issued data write and data read clock signals.

73. A memory subsystem as in claim 68 further comprising a plurality of memory subsystems spaced along said bus and wherein said data write clock signal and data read clock signal have the same period, and wherein said predetermined phase relationship and distance of said memory subsystems from said predetermined location is such that the phase deviation of said data write and data read clock signal at any one of said memory subsystems is less than one half of a data bit time.

Sub A1

74. A memory system as in claim 68 wherein said memory subsystem comprises a plurality of memory storage devices and a data write clock regeneration circuit for regenerating a plurality of data write clock signals from a data write clock received from said bus and respectively providing said regenerated data write clock signals to said memory storage devices.

75. A memory system as in claim 68 wherein said memory subsystem comprises a plurality of memory storage devices, said memory system further comprising a data read clock regeneration circuit for regenerating a plurality of data read clock signals from a data read clock signal received from said bus and respectively providing said plurality of regenerated data read clock signals to said plurality of memory storage devices.

76. A memory system as in claim 75 further comprising a motherboard which contains said bus, said data read clock regenerating circuit being provided at said motherboard.

77. A memory system as in claim 76 wherein said regenerated read data clock signals are generated inside a transmitting device which generates said data write clock signal and data read clock signal.

Sub A1

78. A memory system as in claim 68 wherein said data write signal path is terminated at an end thereof spaced from said memory controller, said memory subsystem being located between said controller and said terminated end, and said data read clock signal path is a loop back signal path.

79. A memory system as in claim 78 wherein said loop back signal path is terminated at an end thereof.

80. A memory system as in claim 78 wherein said loop back signal path terminates at both ends at said memory controller.

81. A memory system as in claim 68 further comprising a plurality of memory subsystems spaced along said bus such that when a data write clock signal and a data read signal are received at each memory subsystem a predetermined minimum time exists between them.

82. A memory system as in claim 81 wherein said predetermined minimum time is about 50% of a data bit time.

83. A memory system comprising:

a data bus comprising a plurality of read/write data paths, a data write clock signal path for propagating a data write clock signal in a first direction

Sub A1

along said bus, and a data read clock signal path for propagating a data read clock signal in a second direction along said bus, said second direction being opposite said first direction;

a memory controller coupled to said bus for respectively issuing said data write and data read clock signals on said data write and data read clock signal paths and for setting a predetermined phase relationship between said data write and data read clock signals at a predetermined location along said bus; and

a plurality of memory subsystems coupled to and spaced along said bus for exchanging data with said memory controller in accordance with timing set by said data write and data read clock signals;

said memory controller setting a phase relationship between said data write and data read clock signals at said predetermined location which ensures that at any one of said memory subsystems a data read operation is not initiated following initiation of a data write operation during a time period which is equal to about 50% of the period of a data bit time.

84. A memory module comprising:

a plurality of memory devices provided on a support structure;

a data write clock line for receiving a data write clock signal; and

a data write clock regeneration circuit coupled to said data write clock line and said memory devices for respectively providing a plurality of regenerated data write clock signals to said memory devices.

85. A memory module as in claim 81 further comprising a register for receiving at least one of command and address signals, the outputs of said register being coupled to said memory devices, said data write clock regeneration circuit providing a regenerated data write clock signal to said register.

86. A memory module as in claim 85 wherein the data write clock signal provided to said register is at a lower frequency than the data write clock signals provided to said memory devices.

87. A memory module as in claim 84 further comprising a plurality of data read clock lines for receiving and providing respective data read clock signals to said memory devices.

88. A bus structure for a memory system comprising:

a plurality of data paths;

a first write clock signal path for propagating a data write clock signal in a first direction along said bus;

a second read clock signal path for propagating a data read clock signal along said bus; and

a data read clock regeneration circuit coupled to said second read clock signal path for regenerating a plurality of data read clock signals from a read clock signal received on said second read clock signal path,

said bus further comprising a plurality of additional read clock signal paths for respectively receiving said regenerated data read clock signals and propagating them in a second direction along said bus, said second direction being opposite to said first direction.